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(54) Title	Prober Device

Abstract

None

Representative drawing

Fig. 3

Specification

[Title of the invention]

Prober Device

[Brief Description of the Drawings]

Fig. 3 is a partial view of a wafer prober device loaded with a test head in accordance with the present invention.

Fig. 4 is a view of another type of test head probe card used in a prober device in accordance with the present invention.

Fig. 5 is a view for illustrating the operation of a wafer prober device in accordance with the present invention.

The present publication includes only main parts, not full content.

(57)Claims

1. A prober device comprising:

a test head means (26) for generating a test signal;

a probe card means (32) being detachably fixed to the test head means (26) and electrically contacting the test piece, whereby inputting the test signal into the test piece in order to test an electrical property of the test piece.

2. The prober device of Claim 1, wherein the probe card means (32) is fixed to the test head means (26) by a screw.

3. A prober device for testing electrical properties of chips formed on a semiconductor wafer comprising:

a probe mechanism (22) provided with a stand (37a) supporting the semiconductor wafer to be tested;

a probe card means (32) provided with an array of probes for testing electrical properties of the wafer by electrically contacting the wafer;

a test head (26) generating test signals by the order of a tester, being detachably fixed to the probe card means (32) and electrically contacting the probe card means (32), whereby the test signals can be input into the wafer via the probe card means (32);

an adjusting mechanism (37) for adjusting the position of the wafer to that of the probe card (32).

4. The prober device of Claim 3, wherein the test head (26) has a performance board (31), the underside of which the probe card (32) is directly fixed to and electrically connected to.

5. The prober device of Claim 4, wherein the performance board (31) is fixed to the probe card means (32) by a screw (33).

6. The prober device of Claim 4, wherein the performance board (31) is fixed to the probe card means (32) by a wire cable (34).

7. The prober device of Claim 4, wherein the performance board (31) is electrically connected to the probe card means (32) by a pogo pin (34).

8. The prober device of Claim 5, wherein the performance board (31) and the probe card means (32) have a contact pad (41) and a contact pad (42) respectively, and the performance board (31) is electrically connected to the probe card means (32) by the electrical contact between these contact pads (41) and (42).

9. The prober device of Claim 3, wherein the adjusting mechanism (37) moves the stand (37a) in a direction of X, Y, Z and θ without moving the probe card means (32).

10. The prober device of Claim 3, wherein the test head (26) is rotatable with respect to the probe mechanism (22) such that the probe card means (32) can contact the wafer when the test head (26) is disposed above the probe mechanism (22).

11. The prober device of Claim 3, wherein the test head (26) has a hole (26a) for receiving a pin electronics board and the hole (26a) has a protrusion at the front end which the probe card means (32) is fixed to.

※ Remark: Published according to the original disclosures.

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(54) 출원명	프로우버 장치		

요약

내용 없음

을 제 3 호 증

대표도

도3

명세서

[발명의 명칭]

프로우버 장치

[도면의 간단한 설명]

제 3도는 본 발명의 데스트 헤드 얹어싣는형 웨이퍼 프로우버 장치를 부분적으로 나타낸 도면.

제 4도는 본 발명의 프로우버 장치에 사용되는 데스트 헤드 프로우브 카아드의 다른 형태를 나타낸 도면.

제 5도는 본 발명의 웨이퍼 프로우버 장치의 동작을 설명하기 위한 도면.

본 내용은 요부공개 건이므로 전문 내용을 수록하지 않았음.

(청구의 범위)

청구항 1.

데스트 신호를 발생하는 데스트 헤드 수단(26)과, 상기 데스트 헤드 수단(26)에 붙이고 떼기가 자유롭게 고정되고, 데스트 피스와 전기적을 접촉함으로써, 상기 데스트 피스에 상기 데스트 신호를 입력하며, 상기 데스트 피스의 전기적 특성을 데스트 하기위한 프로우브 카아드 수단(32)으로 이루어지는 프로우버 장치.

청구항 2.

제 1항에 있어서, 상기 프로우브 카아드 수단(32)이, 상기 데스트 헤드 수단(26)에 나사멈춤 되어 있는 프로우버 장치.

청구항 3.

데스트 해야 할 반도체 웨이퍼를 얹어놓는대(37a)가 형성된 프로우브 기구부(22)와, 상기 웨이퍼와 전기적으로 접촉함으로써 상기 웨이퍼의 전기적 특성을 데스트하기 위한 프로우브 얹이 형성된 프로우브 카아드 수단(32)와 데스터의 지령에 의하여 데스트 신호를 발생하고, 이것을 상기 프로우드 카아드(32)를 통하여 상기 웨이퍼에 입력되는 데스트 헤드(26)로서, 상기 데스트 헤드(26)는, 상기 프로우브 카아드 수단(32)를 붙이고, 떼기가 자유롭게 고정함과 동시에 이것과 전기적으로 접속하고 있고 또한, 상기 웨이퍼와 프로우드 카아드(32)와의 위치 맞춤을 행하기 위한 위치맞춤기구(37)로 이루어져서, 반도체 웨이퍼에 형성된, 칩의 전기적 특성을 데스트 하기 위한 프로우버 장치.

청구항 4.

제 3항에 있어서, 데스트 헤드(26)는, 그의 아래면에, 상기 프로우드 카아드(32)를 직접 고정하고, 이것과 직접 전기적으로 접속하는 퍼포먼스 보오드(31)를 가지는 프로우버 장치.

청구항 5.

제 4항에 있어서, 상기 퍼포먼스 보오드(31)와 상기 프로우브 카아드 수단(32)는, 나사(33)에 의하여 고정되어 있는 프로우버장치.

청구항 6.

제 4항에 있어서, 상기 퍼포먼스 보오드(31)와 상기 프로우브 카아드 수단(32)는, 메탈 커넥팅부재에 의하여 고정되어 있는 프로우버장치.

청구항 7.

제 4항에 있어서, 상기 퍼포먼스 보오드(31)와 프로우브 카아드 수단(32)는, 도고 핀(34)에 의하여 전기적으로 접속되어 있는 프로우버장치.

청구항 8.

제 5항에 있어서, 상기 퍼포먼스 보오드(31)와 상기 프로우브 카아드 수단(32)는, 각각 콘택트 패드(41),(42)를 가지고, 이들 콘택트 패드(41),42)의 접촉에 의하여 상기 퍼포먼스 보오드(31)와 프로우브 카아드 수단(32)가 전기적으로 접촉하는 프로우버 장치.

청구항 9.

제 3항에 있어서, 상기 위치맞춤 기구(37)는, 상기 프로우브 카아드 수단(32)을 이동시키지 않고, 얹어놓는데(37a)를 X,Y,z 및 θ방향으로 이동시키는 프로우버 장치.

청구항 10.

제 3항에 있어서, 상기 데스트 헤드(26)는, 상기 프로우브 기구부(22)의 상부에 대하여 위치 되었을때에 프로우브 카아드 수단(32)가 웨치퍼와 접촉하도록 프로우브 기구부(22)에 회전운동이 자유롭게 설치되어 있는 프로우버 장치.

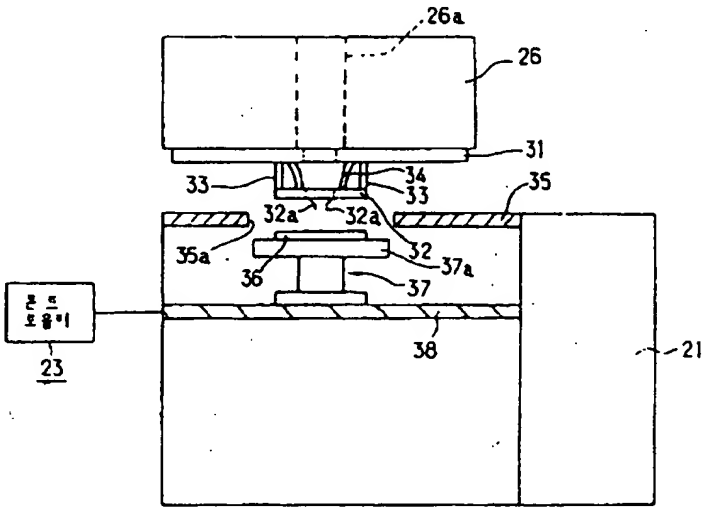
청구항 11.

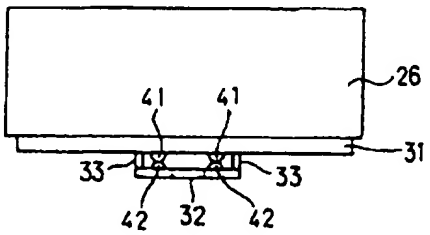
제 3항에 있어서, 상기 데스트 헤드(26)는, 핀 일렉트로닛스보오드를 수용하기 위한 호올(26a)을 가지고, 그 호올(26a)의 앞쪽끝단이 돌출하고, 그 돌출부에 프로우브 카아드 수단(32)가 고정되어 있는 프로우버장치.

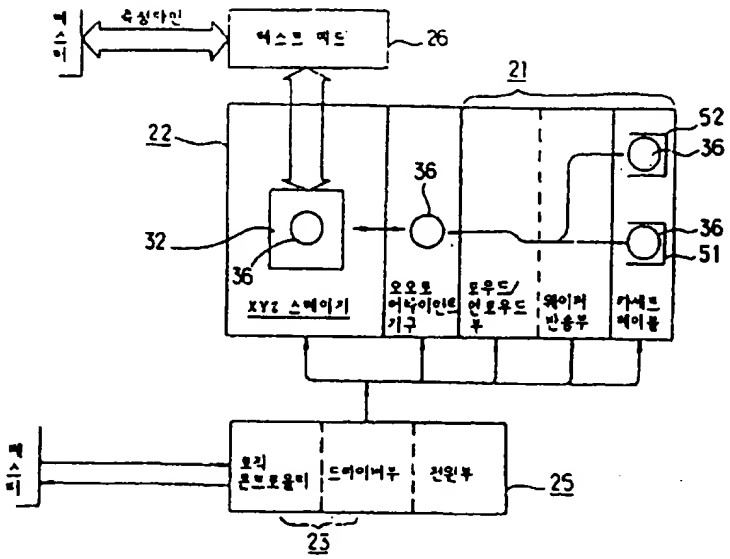
※ 참고사항 : 최초출원 내용에 의하여 공개하는 것임.

도면

도면 3







위 사본임 변호사 민 차 시

2004/4/1

Development of Manufacturing Process for Membrane Probe Card

Research Institute : Korea Institute of Machinery & Materials

Ministry of Science and Technology

SUMMARY

(page 3 to 4 of the Korean text)

I. Title

Development of Manufacturing Process for Membrane Probe Card

II. Objectives

In the manufacturing process for semiconductor, testing IC on the wafer is essential to economical manufacture of ICs. By rejecting defective components at an early stage, unnecessary packaging cost is avoided. The conventional probe card acts as the electro-mechanical interface between the test device and the semiconductor, and transmit the electrical signal between them. Further, the probe card consists of an array of delicate wire contact-styli and a PC board supporting the array. As semiconductor technology advances, IC pin numbers, density and operating speeds increase continually. Today, existing probes have several limitations. One is the distortion of the signal at the test device at high frequency. Another is poor reliability when testing ICs with 256 or more pins.

Membrane probe card has been developed as a solution to these problem and industrialized by Tektronix, Inc. in U.S.A.

As ICs manufacturing technology has been well developed as much as that of advanced country, the demand of membrane probe card is increasing gradually in our industries. However, it is severe that the advanced country does not open the manufacturing technology for membrane probe card. Thus, it is inevitable that the membrane probe card should be developed with our own technology.

This study was carried out for development of membrane probe cards which is high performance and high price of it.

III. Contents

- Development of photo-masking process for fine pattern etching and plating.

- Development of fine plating for bump formation.
- Development of fine pattern etching for formation of microcircuit on the membrane.
- Manufacturing of multi-layered PCB for membrane probe card.
- Development of precision contact mechanism for bumps.

IV. Results and Recommendation

1. Manufacturing process for membrane probe card was developed.
2. Bump, which is essential to manufacture of membrane probe card, was formed with a size of 110μm dia. and pitch of 150μm, and fine pattern of circuit was etched with a line width of 58μm by lithographic technology.
3. Microhardness of bump deposited with a nickel was in the range of Hv 570 to Hv 650 which is similar to that of tungsten. Rhodium deposit is 1.3 times as hard as tungsten and its value is about Hv 891 to Hv 927.
4. Membrane probe card was fabricated as a sample which has a 30 count of bumps and can be used for testing 256K DRAM. It is revealed that the possibility of industrialization. It appears that the probe card such as above sample can replace the tungsten probe card. However, performance test should be carried out for using in the field, and further study is recommended to achieve the high density probe manufacturing as a level (250 pins) of advanced country.

CONTENTS

Chapter 2. Literature Survey

(page 15 to 27 of the Korean text)

Section 1. Conventional Tungsten Probe Card

1. Function

As shown in Fig. 1, circuits are made through semiconductor manufacturing process comprising an element design, VLSI design, production of mask and various repeated manufacturing process on silicon wafer. The manufactured circuits are cut off in the unit of element, and placed on lead frame. After wire bonding, it was packaged by resin or ceramic in order to protect the circuits, and then final products are provided through a final test.

Increasing yield is very important to semiconductor manufacturing. It is necessary to obtain more accurate test result in order to increase yield. If the yield is just increased by 1%, it has much effect on substantial cost reduction because, by previously rejecting defective chips as a result of the test, following process to the defective components can be omitted. The probe card plays an important part in this increase of yield.

A probe card functions as electrical connection between a test device and rectangular-shaped IC pads formed with a size of 10μm on the wafer. Thus, the probe card plays a leading role in the IC test.

As shown in Fig. 2, a blade-typed probe card tests IC chips formed on a wafer in order to detect whether circuits on the wafer function well. IC chips formed on the wafer are shown in a center circle. Ten or more needles (tungsten probes) are electrically contacted with IC pads and transmit electrical signal from a test device to IC pads, and then transmit the response to the test device. Consequently, it can be determined whether the IC under test is defective. Black rod at the center of the circle shown in Fig. 2 marks with a dot to indicate a defective portion in IC. The work in the defective portion is not carried out upon wire bonding because the detect apparatus using a camera can discern the defective portion.

2. Types

The existing probe cards are classified into three groups, i.e., epoxy ring, ceramic blade and metal blade, as shown in Fig. 3. The probes of these probe cards are made by chemically or electrochemically corroding the ends of tungsten lines so as to sharpen the ends like a needle, bending the end portions as shown in Fig. 4, and grinding and flattening the end portions so as to improve contact with IC pads.

The epoxy ring had been initially developed in the 1960's. At the beginning, the combinative assembly, wherein individual probes could be adjusted, was used. However, the introduction of MOS (Metal-Oxide Semiconductor) technique increased the number of probes up to 60, and therefore, made it difficult to practice this method.

The epoxy ring card is made by the following steps: aligning the ends of tungsten needles to a film patterned into IC pads; putting these ends into a ring-shaped epoxy resin; curing the resin; grinding the needle ends so as to have a small plane; and fixing the needles to a printed circuit board (PCB) by soldering.

The blade-typed probe card got its name because metal or ceramic to support a wire probe is soldered on a PCB as a form of a thin plate. In all probe cards of this type, the position and safety of their probes depend on PCB. The support of the ceramic blade has no flexibility and no heat is applied during manufacture. Thus, there is no element causing residual stress after manufacture. Accordingly, the ceramic blade has advantages of less deflection and high safety.

3. Problems

As the conventional probe cards are made of tungsten lines, it is very difficult to align these lines with tens or hundreds of IC pads. The positions of the needles change along with the probing process, and thus, their positions should be frequently adjusted. Further, if the needle ends have poor planarity, contact loads are increased in order to uniformly contact points of all the needles. In this circumstances, scrubbing phenomenon that the needle ends slide on the pads occurs. A normal scrubbing phenomenon removes the protective layer of

SiO_2 applied in the final step of wafer processing process and the oxide layer formed on Al pads, thereby reducing contact resistance. However, an excessive scrubbing phenomenon damages even the Al layer, thereby inhibiting wire bonding, and makes the needles of the probe card slide out of the pads into breakage. Fine Al debris generated by scrubbing cause noises of electrical signals, thereby inhibiting precise test. Due to the above reasons, per 10 to 20 thousand uses, the positions and planarity of the needles should be adjusted and the needle ends should be cleaned. As well, the lifetime of the cards is only 100 to 200 thousand uses.

In fact, the probe cards do not keep up with a recent rapid development of IC manufacture technique. Therefore, the conventional probe cards confront problems in function as well as in efficiency. First, as IC with 500 or more pads is manufactured, the number of probes should increase up to that of pads. However, with the existing tungsten lines, the maximum number of probes is about 256. In addition, it is almost impossible to arrange such number of probes by handwork. Its complexity decreases lifetime, thereby degrading practicability. Second, as IC speed highly increases, a test for processing high-frequency AC (Alternative Current) signals should be performed. However, the conventional tungsten cards have the limits to the frequency, and therefore, cannot perform the test.

Section 2. Membrane probe card

1. Principles

The membrane probe card was initially developed by IBM of U.S.A. in 1968 in order to solve the problems of the conventional probe card.

Fig. 5 shows the basic principles of the membrane probe compared to the conventional probe. The conventional wire probe has the following disadvantages. Its tungsten needles in contact with the pads causes unnecessary electrical induction over 50 MHz in a high-frequency test. As well, the number of pins is limited and the high density of pins results in high cost and damage to IC pads. The membrane probe is manufactured by

using lithography. Instead of tungsten wires, a copper foil is etched on a membrane and circuit lines are made. As a contact point of pin end, a dome-shaped bump is formed at the end of the cooper line by plating. The method by lithography may increase the number of bumps up to 500. Internal impedance may be adjusted by controlling the width of the lines. The bumps are not deflected, and therefore, does not require for adjustment of their positions during manufacture or use, thereby enhancing their lifetime and preventing damage to the pads. As mentioned above, the membrane probe card has solved most of test problems in the conventional probe cards. Even if the membrane probe card has complex configuration, a plurality of probe cards may be easily and repetitively manufactured, thereby producing high density probes at low cost.

2. Structure

The structure of the membrane probe card consists of four important elements, as shown in Fig. 6.

A thin-film-hybrid membrane, a core element of this system, comprises a bump in contact with IC pad, and impedance-controlled circuit lines which are formed to align with the positions of pads. The membrane is precisely manufactured through plating and etching process by using lithography technique. Fig. 7 illustrates a bump-typed and pad-typed contact pad.

A PCB for interfacing is a printed circuit board to perform an intermediate circuit board connecting the membrane to a test device. The PCB also performs a structure to impose loads to make the bump on the membrane in contact with IC pad. In order to maintain the signal system from an interface of test device to a center ring of PCB, the PCB is designed into signal lines whose impedances are controlled. Power, sense and ground lines formed on the hybrid membrane are connected to the wires of the center ring of PCB, and a ground plate extends immediately before the bump.

A transparent, insulated and resilient rubber plate is installed on the back surface of the bump. The rubber plate removes minute differences in planarity of bumps, eliminates contact deficiencies due to differential height between pads, and makes contact pressure

uniform.

A planar plate having fine adjustment screws supports the membrane through the resilient rubber plate and is designed to apply uniform pressure between the plate and a semiconductor. The planar plate is used for coarse adjustment of planarization within 1 to 2 mm.

3. Efficiency

The number of bumps in the currently used membrane probe card is more than 360 and the pitch between the bumps is less than 4 mil (101.1μm). In a near future, a product with 500 or more contact points and a 3 mil (76.2μm) or less pitch may be expectable along with development of manufacture technique. Even if the number of bumps and the density of bumps increase, the bumps do not likely become short one another by misaligning or bending just like wire-used probes because the bumps are fixed on the membrane. Thus, the bumps does not require for adjustment of positions during their lifetime, whereas the conventional probe requires it.

The bumps have about 1.25 times strength as large as that of the existing tungsten material. As shown in Fig. 8, an average 4.5μm wear occurs per a million uses, and therefore, its lifetime is about a million uses. In addition, as shown in Fig. 9, the bumps have a low 0.25ohm contact resistance. From about 150 thousand uses, the resistance value vibrates a little. It is because the debris scrubbed from oxide Al layer begins contaminating the bump surface. Thus, the bumps need to be cleaned only per 200 thousand uses. The bumps have lower contact pressure, 1 g/mil than that of the tungsten probe, 3 to 5 g/mil.

The impedance of the membrane may be controlled by changing width of lines, whereas that of the wire may not be controlled.

In case of using the wire, the high frequency test for AC frequency characteristics may not be performed because about 20nH inductive vortex occurs over 50MHz. To the contrary, in case of using the membrane, an at least 2.0GHz bandwidth and 200ps or less risetime may be obtained. A crosstalk lessens to -35dB, a signal line capacitance is less than 4pF at 50ohm and a mutual capacitance is less than 150fF ($\times 10^{-15}$F).

A settle down time after electrical signals being stabilized is short. Fig. 10 shows data for electrical signal characteristic obtained from the membrane probe.

The membrane probe card is manufactured by lithography technique similar to that applied to wafer fabrication. The membrane probe card is used as a VHD wafer probe card for testing a high efficiency IC with a large number of pins including gate array, semi- or full-custom application-specific IC (ASICS), custom logic, and VLSI semiconductor.

The VHD probe card is suitable for probing GaAs, ECL, CML and high speed CMOS semiconductor, and other semiconductors with an 1V/ns or more slew rate.

4. Economical efficiency

The price of the membrane probe card is a little higher in the basic manufacturing costs, because the manufacturing process itself is completely different from that of the convenient probe card. For example, for 60 pins, the price of membrane probe is approximately 11,000 dollars, whereas, the convenient probe is 400 dollars. However, for 240 pins, the price of the membrane probe card is increased by 50% to 15,950 dollars, although the pin number is increased by 4 times, whereas, the price of the tungsten probe is increased by 7.5 times to 3,000 dollars. Also, refer to C. Barsotti, etc. of Tektronix Inc., the price of the probe card is 200 dollars for 24 pin and 10,000 dollars for 360 pin. Therefore, it is noted that the price per pin is increased, i.e. 6 dollars per pin for low density and 12.5 dollars per pin for high density, except the price of PCB and the assembling cost. Now, the price of the membrane probe card is extremely higher than that of the convenient prove card. However, it is expected that in the future the membrane probe card would be advantageous in the prices and should be used in view of the performance.

The improvement of the probe card can enhance the yield by 1~5%. In the factory where one million of 5 dollars semiconductors are produced per month, only 1% of the yield enhancement can increase the sales by 600,000 dollars per year. The decrease in the product cost is considerable if inferior goods could be removed previously, because the packaging

cost of recent high-density IC may be up to 100~500 dollars.

Chapter 3. Contents

(page 28 to page 30, line 5 of the Korean text)

Section 1. Manufacturing process

A membrane probe card (MPC) is composed of 4 major elements, i.e. a membrane, a printed circuit board (PCB) for supporting the membrane, a planarity adjustment plate, and a transparent elastic rubber plate.

These elements are manufactured through a series of necessary manufacturing process for each element. Then, a final product is manufactured by assembling these elements. Fig. 11 shows a manufacturing process flow chart for the membrane probe card.

First, IC for applying MPC is selected. Then, the elements for manufacturing MPC where the suitability test for IC is performed are designed. In order to form bumps which are contact points, a film substrate having necessary area for reading the coordinates of the locations of the IC pad are manufactured.

This film substrate is located on the membrane PCB coated by photoresist agents. Then, masking is achieved by exposing light and developing, except the locations for bumps plating. After forming the bumps, photo resist is removed. In order to make circuits which are signal connecting lines between the bumps and the PCB plate, the membrane is masked by a circuit substrate film like the above-mentioned bumps forming methods, and then the circuit substrate film is etched, thus finally fabricating accurate circuits.

On the other hand, the PCB is manufactured by applying conventional dry film masking, various plating processes, and etching process on the PCB board which serves as a frame for supporting the membrane and connects the membrane with a test apparatus.

The membrane probe and the terminals of the PCB are connected by tape attachment method or mechanical heating and pressing method. The solid planarity adjustment plate, which can adjust planarity by using four screws, is assembled. The transparent rubber plate

is inserted between the membrane and the solid planarity adjustment plate, thus being assembled into a final product. The transparent rubber plate is for removing the minute height differences among the bumps.

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(page 53, line 3 to page 58 of the Korean text)

7. PCB board and planarity adjustment plate

A. PCB board

PCB board is annular disk shaped with a central circular aperture such that the membrane probe is installed. Its functions are supporting the membrane probe and interfacing the signals from the probe with the testing apparatus. Also, it functions as a structural member for the entire probe card such that the bumps are maintained horizontally and the planarity adjustment plate can be attached.

PCB board is manufactured in the sequence of manufacturing process shown in Fig. 28. The required plating process is achieved with the common commercial plating agents and the conditions thereof. Masking process is achieved by the same method as the above-mentioned dry fill using process. Laminating is achieved using Vacuum Laminator purchased by the research fund, in order to improve the accuracy of the circuit. Fig. 29 shows the film used for manufacturing PCB board, (a) shows the film for circuit fabrication, and (b) shows the film for solder masking of hole portions. Fig. 30 is a photograph of the two-sided PCB board for the probe card having 120 terminals.

B. Planarity adjustment plate

The planarity adjustment plate is installed on the membrane opposite to the bumps. The planarity adjustment plate is accurate disk shaped with 4 fine control screws for

supporting the membrane and uniformly imposing contact pressure upon testing. The material is high quality bakelite which can be treated accurately in the order of μ *m*. To observe the locations of the probe upon testing, the circular aperture of 10mm diameter are located on the center of the disk.

8. Assembling of prototype

Fig. 31 is a cross sectional view of the prototype assembling the membrane probe, the PCB board, the planarity adjustment plate, and the transparent elastic rubber plate which are manufactured by the above-mentioned process.

The planarity adjustment plate is assembled by 4 fine control screws with the PCB board on which circuits are formed. In the central circular through hole, the transparent elastic silicon rubber plate is installed on the back side of the membrane, and a transparent acryl substrate is simultaneously inserted and assembled, in order to equalize the contact pressure differences resulted from the height differences among the bumps or among the pads.

The membrane is formed in the manner of bending up the outskirts of the bumps, in order that only the bump portions are contacted. This process is achieved by applying pressure to the membrane on a heated die. The bent membrane is attached to a bakelite bottom plate by applying adhesive agents. The circuit terminals of the membrane are connected to the end of the PCB terminals by heating to 120 ℃ and pressing, using Zebra tape.

Through the above mentioned process, the prototype membrane probe card for testing 256K DRAM is manufactured. The prototype membrane probe card has 30 bumps, and the size of bump is 150 μ *m*.